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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/197,314
Filing Date: November 20, 1998
Appellant(s): KRISHNAMACHARI, SANTHANA

Russell Gross
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 6, 2003 appealing from the Office action mailed September 18, 2002.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affect by or have a bearing on the decision in the pending appeal is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of the Invention

The summary of the invention contained in the brief is correct.

(6) Issues Presented for Review

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: The statement "The first issue is whether Claims 1-6, **8**-19, 22-26, 40, and 45-46 under 35 USC 102 are anticipated by Ueno et al" as shown at page 3 of the Brief should be "The first issue is whether Claims 1-6, **9**-19, 22-26, 40, and 45-46 under 35 USC 102 are anticipated by Ueno et al".

(7) Grouping of Claims

The appellant's brief includes a statement that the claims either stand or fall together.

(8) Claims appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,418,570	UENO ET AL	5-1995
5,475,435	YONEMITSU ET AL	12-1995
6,091,777	GUETZ ET AL	7-2000
6,163,576	LEMPEL	12-2000
6,115,070	SONG ET AL	9-2000.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 9-19, 22-26, 40, 45, and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueno et al of record (5,418,570).

Ueno et al discloses a motion picture coding apparatus as shown in Figures 1, 7, 13, 15, and 18-21, and the same apparatus, method, and computer executable process steps stored on a computer readable medium as claimed in claims 1-6, 9-19, 22-26, 40, 45, and 46, the computer

executable process steps to increase a resolution of at least a portion of a reference frame of video (see 35 of Figures 7 and 13, 60 of Figure 15), the apparatus, method, and computer executable process comprising the same selecting a first block of pixels in the reference frame (see columns 1-2, column 15, lines 33-41, column 16, lines 8-20); locating in N target frames one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame (i.e., search range calculation within coding section 30 of Figures 7 and 13, see column 15, lines 33-41); determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks, adding the additional pixels among the pixels in the first block, determining the values of the additional pixels based also on coefficients which are weighted in accordance with the first block and the one or more blocks, wherein the coefficients are weighted based on differences between pixels in the first block and pixels in each of the one or more blocks, wherein the differences comprise a residual (i.e., 35 of Figures 7 and 13, 60 of Figure 15, Figures 18-21, and see columns 1-2, columns 7-8, columns 15-16, columns 19-21); wherein the N target frames comprise frames of video which were predicted at least in part based on pixels in the reference frame (see column 16, lines 8-20); wherein in a case that the locating step does not locate any blocks of pixels in the target frames that substantially correspond to the first block of pixels, the determining step determines the values of the additional pixels based on values of pixels in the first block without regard to values of pixels in the N target frames (i.e., I frame processing, see column 2, lines 31-39); changing distances between pixels in the first block in order to change a size of the first block (see Figures 18-21, column 19-21); wherein the locating step uses motion vectors from the reference frame to the target frame to locate the one or more

blocks of pixels and searches through the N target frames to locate the one or more blocks of pixels (see column 15, lines 33-41); the locating step locates one or more blocks using motion vectors present in an coded bitstream for target frames and wherein the coefficients are determined using DCT values of at least one coded residual, where the at least one coded residual comprises differences between the reference frame and the target frames (see column 15, lines 33-41, column 20, lines 54-68, Figures 7, 13, 15, 18-21); and wherein the reference frame comprises a B frame, and wherein before the selecting step, the step of determining a location of the first block in the reference frame based on blocks of pixels in frames which precede and which follow the reference frame (i.e., bidirectional prediction, see column 16, lines 8-20); and wherein the reference frame comprises one of an I frame and P frame, and wherein the N target frames comprise at least one of a P frame and a bi-directional frame (see column 2, lines 31-39, column 16, lines 8-20).

3. Claims 42 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonemitsu et al of record (5,475,435).

Yonemitsu et al discloses a layer encoding and decoding apparatus as shown in Figures 1 and 2, and the same television system which receives coded video data (see column 1 and Figure 2), and which forms images based on the coded video data, the television system comprising a decoder (see Figure 2) which decodes the video data to produce frames of video; a processor (55, 57 of Figure 2) which increases a resolution of a reference frame of video based on pixels in the reference frame and based on pixels in at least one other target frame of the video, wherein the processor increases the resolution of the reference frame by selecting blocks of pixels in the reference frame and for each selected block, locating in N target frames one or more blocks of

pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame (see column 2, lines 44-54, column 3, lines 25-35, column 4, lines 53-63, column 6, line 34 to column 7, line 63), and determining values of additional pixels based on values of pixels in the selected block and on values of pixels in the one or more blocks and adding the additional pixels among the pixels in the selected block (i.e., interpolation within upsampling circuit 57 of Figure 2); a display which displays an image based on the reference frame (see column 1 and Figure 2); and wherein in a case that the processor does not locate any blocks of pixels in the target frames that substantially correspond to the selected block of pixels, the processor determines the values of the additional pixels based on values of pixels in the selected block without regard to values of pixels in the N target frames (i.e., I frame processing as determined from the macroblock type signal, see column 2, lines 55-62, column 6, lines 34-44).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al as applied to claims 1-6, 9-19, 22-26, 40, 45, and 46 in the above paragraph (2), and further in view of Guetz et al of record (6,091,777).

Ueno et al discloses substantially the same apparatus, method, and computer executable process steps as above, but does not particularly disclose determining the values of the additional

pixels by performing bilinear interpolation using at least some of the pixels in the first block as claimed in claims 7 and 20. However, Guetz et al discloses a continuously adaptive digital video compression system and teaches the conventional use of bilinear interpolation associated with motion estimation of blocks (see column 2, lines 23-47). Therefore, it would have been obvious to one of ordinary skill in the art, having the Ueno et al and Guetz et al references in front of him/her and the general knowledge of the interpolation of images, would have had no difficulty in providing the bilinear interpolation of image data as taught by Guetz et al as part of the motion estimation of pixel data within the system of Ueno et al for the same well known image interpolation purposes as claimed.

6. Claims 27-32, 35-39, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al as applied to claims 1-6, 9-19, 22-26, 40, 45, and 46 in the above paragraph (2), and further in view of Lempel of record (6,163,576).

Ueno et al discloses substantially the same apparatus, method, and computer executable process steps as above, but does not particularly a memory which stores computer executable process steps as claimed in claim 27. However, Lempel discloses a video encoder having reduced memory bandwidth requirements, and teaches the conventional use of a CPU 202 of Figure 2 for storing and executing computer processes. Therefore, it would have been obvious to one of ordinary skill in the art, having the Ueno et al and Lempel references in front of him/her, would have had no difficulty in providing the computer memory storage of executable processes as taught by Lempel for the video image processing system of Ueno et al for the same well known purposes as claimed.

7. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ueno et al and Lempel as applied to claims 1-6, 9-19, 22-32, 35-40, and 45-47 in the above paragraphs (2) and (6), and further in view of Guetz et al of record (6,091,777).

The combination of Ueno et al and Lempel discloses substantially the same apparatus, method, and computer executable process steps as above, but does not particularly disclose determining the values of the additional pixels by performing bilinear interpolation using at least some of the pixels in the first block as claimed in claim 33. However, Guetz et al discloses a continuously adaptive digital video compression system and teaches the conventional use of bilinear interpolation associated with motion estimation of blocks (see column 2, lines 23-47). Therefore, it would have been obvious to one of ordinary skill in the art, having the Ueno et al, Lempel, and Guetz et al references in front of him/her and the general knowledge of the interpolation of images, would have had no difficulty in providing the bilinear interpolation of image data as taught by Guetz et al as part of the motion estimation of pixel data within the system of Ueno et al for the same well known image interpolation purposes as claimed.

8. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemitsu et al as applied to claims 42 and 43 in the above paragraph (3), and further in view of Song et al of record (6,115,070).

Yonemitsu et al discloses substantially the same television system as above, but does not particularly disclose wherein the decoder and the processor are implemented in a settop box as claimed in claim 44. Such decoder and processing within a settop box is however old and well recognized in the art, as exemplified by Song et al (See Figure 24 and column 24, line 64 to line 18. Therefore, it would have been obvious to one of ordinary skill in the art, having the

Yonemitsu et al and Song et al references in front of him/her and the general knowledge of settop box functions, would have had no difficulty in providing the settop box with decoder and processing capabilities as taught by Song et al for the video image system of Yonemitsu et al for the same well known MPEG compliant decoding purposes as claimed.

(11) Response to Argument

Regarding the appellant's arguments at pages 4-7 of the Brief filed February 6, 2003 concerning in general that "... the burden of showing that Ueno et al anticipates all of the features recited in the claims has not been met. In particular such features include "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as recited in claims 1, 14, 27 and 40. Initially, in addressing this feature in the above rejections, the upsampling circuit 35 shown in Figure 7 of Ueno et al is being relied on ... the Appellant has carefully reviewed the above portions and does not see where it supports the above interpretation of Ueno et al ... Moreover, in column 19, lines 41-54, Ueno et al discloses a signal obtained by horizontal up-sampling ... is separated into an odd-field signal and even-field signal in the first field separator 402 ... Based on the above disclosure, it is evident that the up-sampling of Ueno et al does not perform "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as required by the claims ...", the Examiner respectfully disagrees. It is submitted again that the low resolution local decoded signal 34 output from the local decoder 33 as shown in Figure 7 of Ueno et al is actually based on first blocks of pixels in the reference frame and one or more blocks of pixels that substantially correspond to the first block of pixels as provided by the search range calculation within coding section 30 of Figure 7 of Ueno et al (see column 8, line

41 to column 9, line 34, column 12, line 35 to column 13, line 60, column 14, lines 33-41, column 15,m lines 33-41, column 16, lines 8-20). The low resolution local decoded signal is further upsampled by upsampling circuit 35 of Figure 7 of Ueno et al (see also Figure 15), thereby adding pixels to the low resolution local decoded signal (see columns 19-20 and Figure 18). The appellant's attention is further directed to Figure 18 and column 19, lines 26-34 of Ueno et al for the particular teachings of a low resolution picture provided to upsampling circuit 60 so as to be doubled in the horizontal direction, and is then subjected to vertical upsampling. This doubling in the vertical and horizontal directions therefore provides additional pixels to the low resolution picture, in order to produce an upsampled picture. This basic horizontal and vertical direction upsampling of a low resolution picture is also depicted at Figure 3A of Ueno whereby a 2x2 low resolution picture is upsampled to produce a 4x4 picture. The horizontal upsampling as argued by the appellant is nevertheless part of the process of producing additional pixels to the low resolution picture, since Ueno teaches at column 19, lines 26-34 that the low resolution local decoded signal is upsampled to be doubled in the horizontal direction. As such, it is submitted that upsampling circuit 35 of Figure 7 of Ueno et al shows the same "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks" as claimed.

Regarding the appellant's arguments at pages 7-8 of the Brief filed February 6, 2003 concerning in general that "... However, in this portion, Ueno et al only discloses that an odd field and even field signal are subjected to a vertical interpolation. Based on this disclosure, it is evident that individual fields are only being interpolated. Thus, it is unreasonable to interpret this as "determining values of additional pixels based on values of pixels in the first block and on

values of pixels in the one or more blocks", as required by the claims ...", the Examiner wants to point out that such arguments have been addressed in the above paragraph. But, the Examiner wants to add that similar to the horizontal upsampling process, the vertical upsampling process for interpolation of the odd and even field components provides the addition of pixels to the low resolution local decoded signal, as exemplified in Figures 3A and 18 of Ueno et al.

Regarding the appellant's arguments at pages 8-10 of the Brief filed February 6, 2003 concerning in general that "... it is also respectfully submitted that the burden of showing that Yonemitsu et al anticipates all of the features recited in the claims has not been met. In particular, such features include "a processor which increases a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as recited in claim 42 ... However, in column 7, lines 11-13, Yonemitsu et al clearly discloses that the output picture S66 of the lower layer is input to the up sampling circuit 57, in which it is processed by interpolation so that its converted into a non-interlace picture. Based on this disclosure, it is evident that only a single picture is interpolated. Thus, it is evident that the up sampling circuit 57 of Yonemitsu et al does not "increase a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as required by the claims ...", the Examiner respectfully disagrees. It is submitted again that since the upsampling circuit 57 of Yonemitsu et al performs an interpolation of picture data, such interpolation will provide an increase in resolution of the picture. And since the motion compensation decoding 55 of Figure 2 of Yonemitsu et al decodes the motion vector provided by the motion estimation process of the encoder (see column 2, lines 44-54, column 3, lines 25-35, column 4, lines 53-63, column 6, line 34 to column 7, line 63), one

or more blocks of pixels from the target frames are being located that substantially corresponds to the first block of pixels. The lower layer picture S66 as provided to the upsampling circuit 57 of Yonemitsu et al is based on the motion compensated data from motion compensation decoder 55 (see column 6, line 34 to column 7, line 15), and as such it is therefore submitted that the interpolation process provided with in the upsampling circuit 57 provides the same increase of resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of video (i.e., as provided by the motion estimation and compensation decoding process) as claimed.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Richard Lee/rl

December 2, 2005

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